First Prototype of a Machine Learning Trigger Algorithm on FPGA for Micromegas detectors

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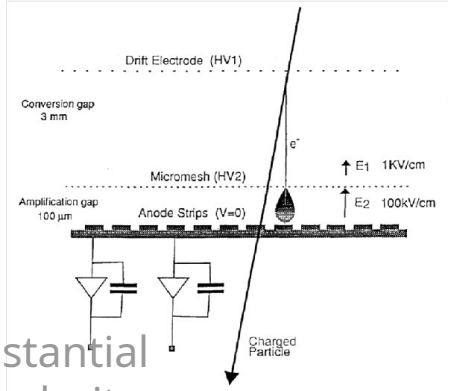
Background Substraction for Radiation Detectors

Key points

Each radiation detector is affected by background radiation leading to a loss in detector efficiency. The background substraction is an old problem that requires new approaches.
We present the work performed for Micromegas detectors applied for muon detection but this approach can be applied to any type of similar scenarios.
We use a geometrical approach in detection of unwanted events.

Micromegas Detector in our setup



Key points

> The design of Micromegas is offering, for several applications, substantial advantages in energy, space and time resolution, microscopic granularity on large surfaces, insensitivity to discharges, simplicity of construction and capacity to identify and reduce some sources of background, which can be of great interest in the search for rare events

G Charpak et. al. Micromegas, a multipurpose gaseous detector, DOI: 10.1016/S0168-9002(01)01713-2

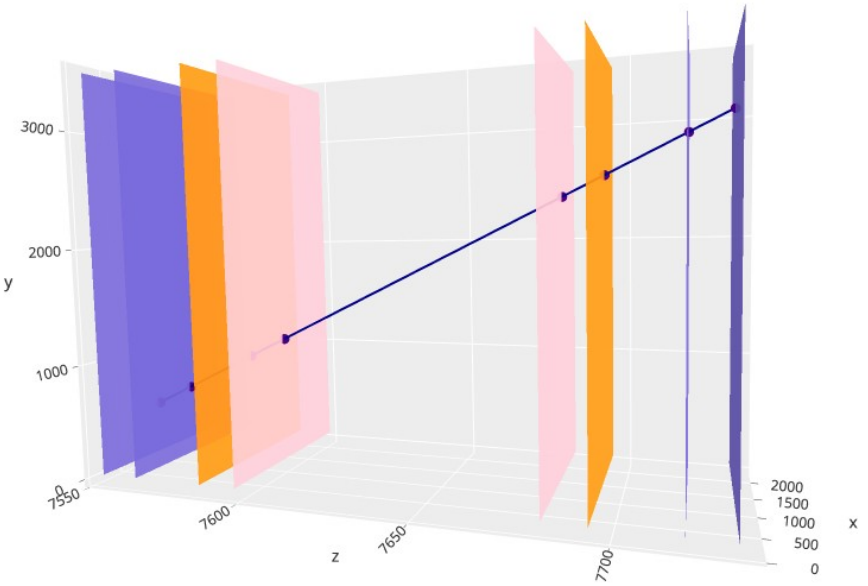
Micromegas Detector in our setup

The Challenges

Output of Δθ
Complex detector setup
- 8 layers muon detector
- 8800 microstrips per detector layer

High data througoutput for detector data
- 8800 x 8 detector image each microsecond

Small processing time Window
- Processing should be done under 1 microsecond
- Accuracy is a key point

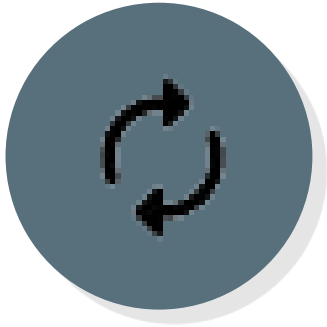


Possible approaches

All prroaches use Field Programable Gate Arrays due the timing constraints.

RTL

Register Transfer Level implemented using Verilog or VHDL
Low level Digital Electronics Blocks



HLS

High Level Synthesis Implemented using high level programming languages (C/C++) converted to RTL

ML

Machine Learning Implemented using regressor networks using FPGA based accelerator cards

Our approach

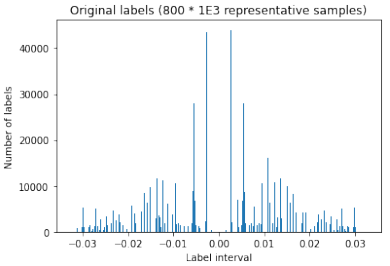
Previous work

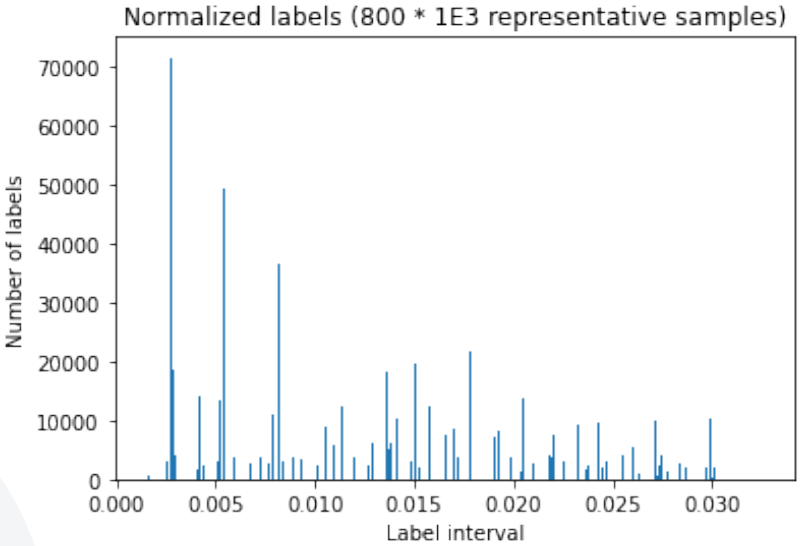
This work is based upon the approach presented in the paper:

I.-M. Dinu, I. S. Trandafir, C. Alexa, A Machine Learning Based Muon Trigger Algorithm for an Assembly of Micromegas Detector, Romanian Journal in Physics, Vol. 67, No. 7-8, 2022

Our work extends this work by implementing the regression models using VITIS-AI framework on Xilinx Alveo U280-PQ card.

The dataset





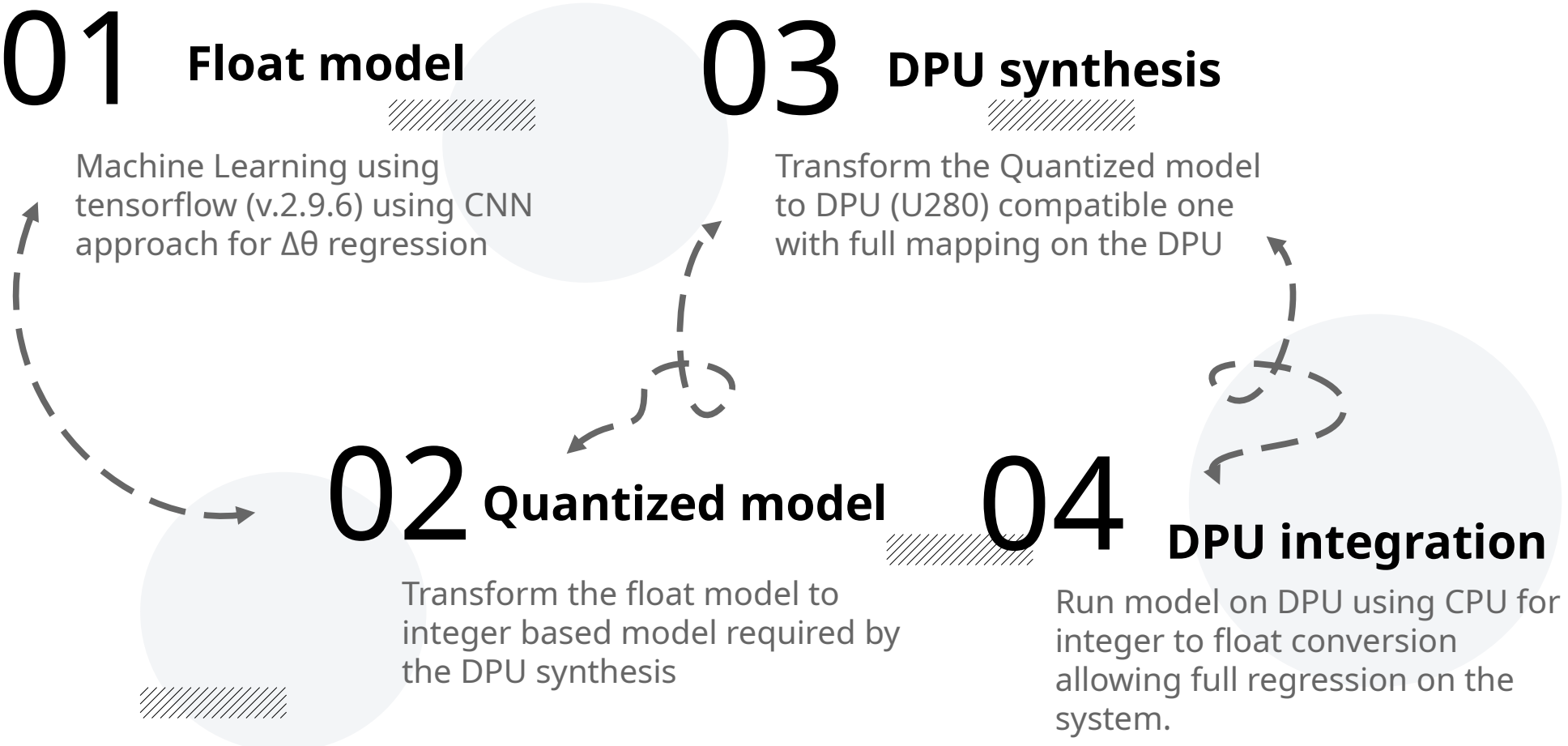
Dataset features

The whole dataset consists of 500M records
- 400.000.000 training records
- 50.000.000 testing records
- 50.000.000 validation records

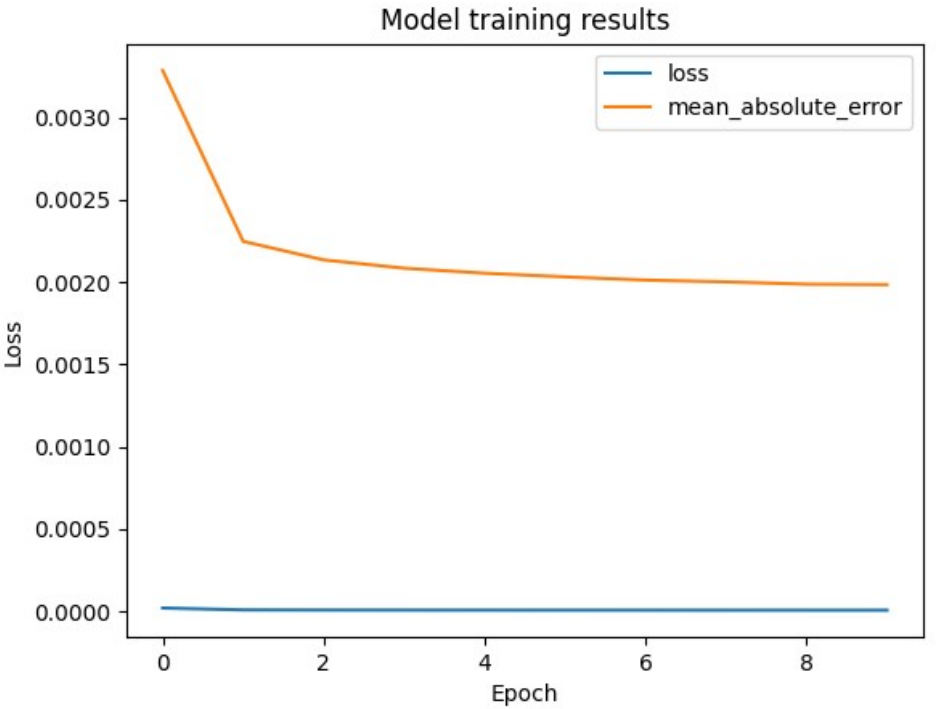
The whole dataset has a considerable size
- Greater than 272 Gb

The data has been normalized

Processing Pileline



Model Development



Model details

The model is developed
- Tensorflow 2.0
- Vitis-AI 2.0
- GPU training takes 10 times less Nvidia Telsa V100S-PCIE-32GB

Float Model Precission:
- MSE: 6.0924e-06 / MAE: 0.0018

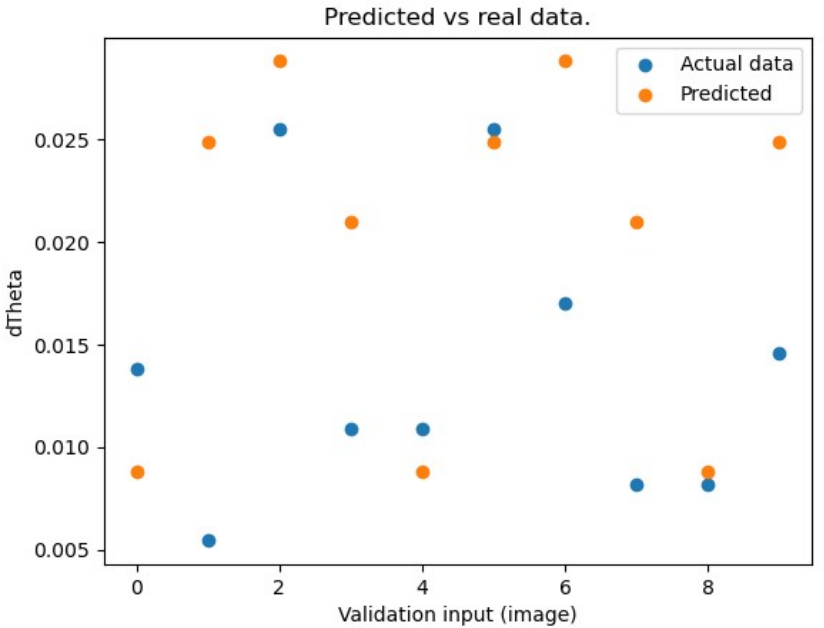
Quantized Model Precission
- MSE: 9.8394e-06 / MAE: 0.0024

Model Development

DPU Synthesis

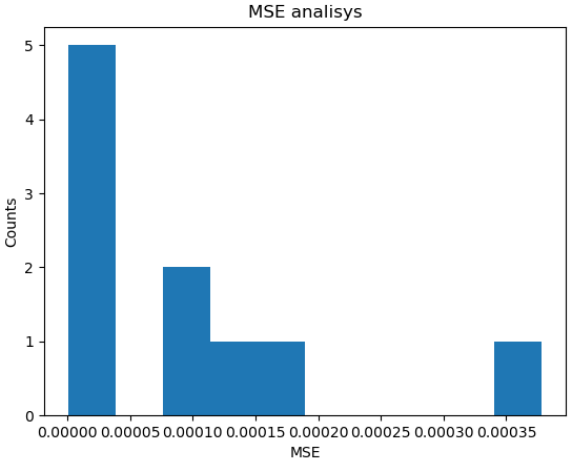
Using Vitis-AI 2.0
Not all layers can be mapped to DPU
Not mapped layers run on CPU (IP)
It’s compiled using Xilinx Tools
Uses XIR (Xilinx Intermediary Representation)
Can be mapped to DPU v3e (1.4) of U280 cards

Results



DPU Inference Preliminary Results

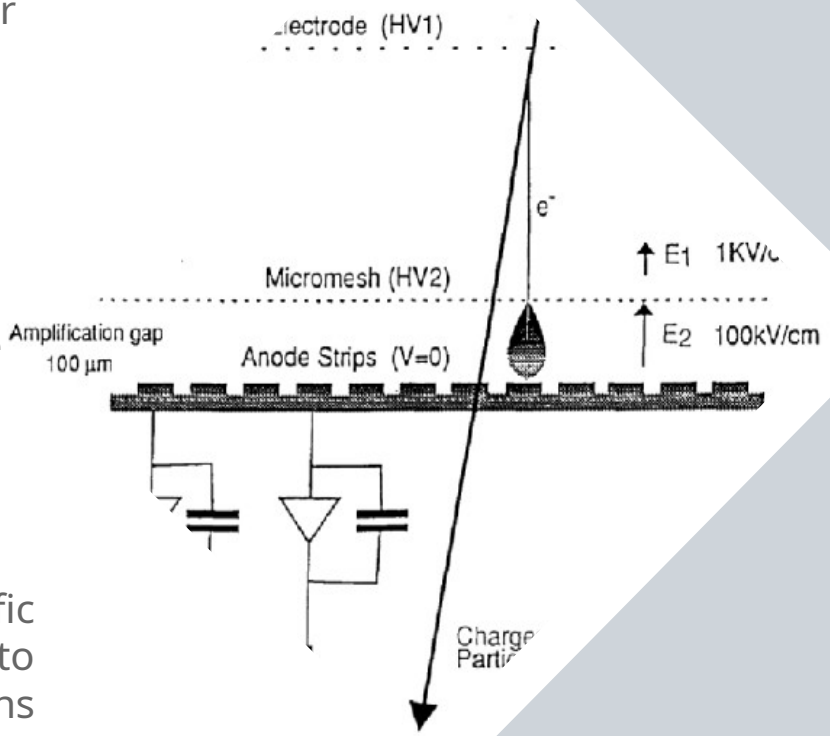
Mean Quared Error (MSE): 9.3e-5
Mean Absolute Error (MAE): 7.61e-3
Debug symbols slow down the model
CPU i/o reduces processing time



Conclusions and Future developments

We have implemented using FPGA based DPU system U280 the trigger processor algorithm prototype using a Machine Learning approach for background discrimination applied for Micromegas multi-layer detector systems.
FPGA mapping is a challenging and iterative problem for ML regression algorithms due the dynamic nature of the technology with great potential for high speed data processing environments.
The simplified model shown today allows for Δθ evaluation with and big error so one of the steps we are working on are to future improve the model.
All CPU layers have to mapped to IP (Intellectual Property) directly on the FPGA board.

Timing considerations provide us with specific restrictions to the implemented model leading to specific RTL/HLS optimizations



Bibliography

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A. Ushiroyama, et. Al. , "Convolutional neural network implementations using Vitis AI," 2022 IEEE 12th Annual Computing and Communication Workshop and Conference (CCWC), 2022, pp. 0365-0371, doi: 10.1109/CCWC54503.2022.9720794.